Institution: Liverpool John Moores University (LJMU)		
Unit of Assessment: Sub-panel 12: Engineering		
Title of case study: Knowledge-based service and design for reliable and secure microelectronic products		
Period when the underpinning research was undertaken: from 2000 to 2020		
Details of staff conducting the underpinning research from the submitting unit:		
Name(s):	**Role(s) (e.g. job title):**	**Period(s) employed by submitting HEI:**
Prof. Jian Fu Zhang	Professor (Group leader)	SL 1992-1996, R 1996-2001, Prof 2001-date
Dr. Zhigang Ji	Reader (R)	SL 2011-2018, R 2018-2019
Prof. Weidong Zhang	Professor (Prof)	SL 2005-2010, R 2010-2014, Prof 2014-date
Dr. John Marsland	Head of Department	Head of Department 2016-date
Dr. Brahim Benbakhti	Senior Lecturer (SL)	PDRA 2011-2013, SL 2013-date
Period when the claimed impact occurred: from August 2013 to December 2020		
Is this case study continued from a case study submitted in 2014? N		

1. Summary of the impact

The research of the Microelectronics Group (MG) has impacted the industry in four ways: (W1) The predicative model developed by the MG has been used for both process qualification and 'product design kit' software; (W2) The developed test techniques have been embedded into commercial instruments as a standard module; (W3) Direct participation in the world-leading industrial consortium that is developing state-of-the-art future technologies; (W4) The in-depth knowledge gained on device instability has been innovatively utilised to design and build a new hardware True Random Number Generator (TRNG) for IoT security applications.

2. Underpinning research

Electronic products can fail. Metal-oxide-semiconductor field effect transistors (MOSFETs) are used in over 90% of integrated circuit chips in electronic products. The oxide and its interface with the semiconductor is at the heart of MOSFETs, and are vulnerable to stresses. Their wear-out rate determines device lifetime. Moreover, wear-out is a stochastic process and contributes to device-to-device variations, which is a major challenge for designing modern chips.

Recognizing the importance of a stable oxide/semiconductor structure to the industry, the Microelectronics Group (MG) has focused their research on this aspect, mainly through six EPSRC funded projects [G1-G6] between 2000 and 2020. The research has been carried out in collaboration with a range of industrial partners, from international leaders such as ARM Ltd and Synopsys, to start-ups such as Semiwise.

The milestones and achievements that underpin this impact case are summarised in chronological order below:

1. A framework has been established for defects, that clearly identifies what kinds of traps exist in the device [G1*, R1*, G2]. In addition to as-grown traps formed during device fabrication, MG's works clearly show that stresses generate new traps.
2. The key properties of each type of defect have been obtained by developing novel measurement techniques. For example, a new energy profile probing method is developed to identify the energy location of traps [G3, R2]. It is found that the generated traps have different energy levels from the as-grown traps and this difference allows an accurate separation of one from the other.
3. Different kinetic models were developed for different type of defects. This breaks the mind-set of early works that all defects follow the same kinetics and leads to the proposal of the 'As-grown-Generation model (AG)'. The industrial standard, JEDEC, uses power-law for ageing kinetics, but test data of modern devices do not follow it, which has puzzled the community. For the first time, MG's works identified the source of this deviation, proposed a method to restore the power-law, and verified that the prediction of the AG model for device ageing under usage conditions [G4, R3].

4. Fast test techniques have been developed for extracting model inputs [G4, R3] to facilitate the application of the proposed model in industrial test laboratories.
5. The application and extension of the knowledge, model, and techniques to qualify new processes, materials, and devices, for example, Resistive Random Access Memory (RRAM) [G5, G6, G7, R4, R5].

The AG model was directly used in predictive modelling, the impact W1, described in the summary. The test techniques developed were embedded in standard instruments (W2). The in-depth knowledge gained and the expertise in testing has enabled the MG to contribute to the development of new technology (W3). This knowledge on defects also led to the design and build of a True Random Number Generator (TRNG) (W4) [G8, R6].

*G and R stand for Grants and Research outputs in Section 3.

3. References to the research

Projects/Grants (G) and Research outputs (R) cited in Sections 2 and 4 are listed below. A research output is placed directly under the grant that funded it.

[G1] Hole Trap Generation and It's Role In Oxide Breakdown, EPSRC, GR/R10387/01, 2001 2004 (£165,961), PI: J. F. Zhang.

[R1] J. F. Zhang, C. Z. Zhao, A. H. Chen, G. Groeseneken and R. Degraeve, “Hole traps in silicon dioxides --- Part I: Properties,” IEEE Trans. Electron Dev., Vol.51, No.8, pp.1267-1273, 2004 (doi.org/10.1109/TED.2004.831379).

[G2] Performance, degradation and defect structure of MOS devices using high-k materials as gate dielectrics, EPSRC, EP/C003071/1, 2005-2008 (£191,097), PI: J. F. Zhang.

[G3] High permittivity dielectrics on Ge for end of Roadmap application, EPSRC, EP/I012966/1, 2011-2014 (£462,589), PI: J. F. Zhang, CoI: W. Zhang.

[R2] S. F. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, “Energy distribution of positive charges in gate dielectric: probing technique and impacts of different defects,” IEEE Trans. Electron Dev., Vol. 60, No. 5, pp. 1745-1753, 2013 (doi.org/10.1109/TED.2013.2255129).

[G4] Time-Dependent Variability: A test-proven modelling approach for systems verification and power consumption minimization, EPSRC, 2014-2018 (£517,676), PI: J. F. Zhang, CoI: Z. Ji and W. Zhang.

[R3] R. Gao, Z. Ji, A. B. Manut, J. F. Zhang, J. Franco, S. W. M. Hatta, W. D. Zhang, B. Kaczer, D. Linten, and G. Groeseneken, “NBTI-Generated Defects in Nanoscaled Devices: Fast Characterization Methodology and Modeling,” IEEE Trans. Electron Dev., Vol. 64, No. 10, pp.4011-4017, 2017 (doi.org/10.1109/TED.2017.2742700).

[G5] Mechanisms and Control of Resistive Switching in Dielectrics, EPSRC, EP/M006727/1, 2015-2018 (£350,016), PI: W. Zhang, CoI: J. F. Zhang.

[G6] Variability-aware RRAM PDK for design based research on FPGA/neuro computing, EPSRC, 2018-2021 (£378,364), PI: W. Zhang; CoI: J. F. Zhang and Z. Ji.

[R4] F. Hatem, Z. Chai, W. Zhang, A. Fantini, R. Degraeve, S. Clima, D. Garbin, J.Robertson, Y. Guo, J. F. Zhang, J. Marsland, P. Freitas, L. Goux, G. S. Kar “Endurance improvement of more than five orders in GexSe1-x OTS selectors by using a novel refreshing program scheme,” Technical Digest of the International Electron Devices Meeting (IEDM), pp. 827-830, San Francisco, Dec. 7-11, 2019.

[R5] D. Joksas, P. Freitas, Z. Chai, W.H. Ng, M. Buckwell, C. Li, W.D. Zhang, Q. Xia, A.J. Kenyon, A. Mehonic, “Committee machines—a universal method to deal with non-idealities in memristor-based neural networks,” Nature Communications, Vol. 11, Article number: 4273, 2020 (doi.org/10.1038/s41467-020-18098-0).

[G7] Rolling research collaboration project with IMEC: Euro100k p.a. since 2005

[G8] A true random number generator (TRNG) MVP for RFID tags in healthcare, Innovate UK, 2018-2019 (£109,952), PI: Z. Ji.

[R6] J. Brown, R. Gao, Z. Ji, J. Chen, J. Wu, J. F. Zhang, B. Zhou, Q. Shi, J. Crowford, and W. Zhang, “A low-power and high-speed True Random Number Generator using generated RTN,” Proc of IEEE VLSI Tech. Symp., pp. 95-96, Honolulu, June 2018.

4. Details of the impact

The research of the Microelectronics Group (MG) is mainly funded by the EPSRC. EPSRC emphasizes the impact of research on industry and society. MG shares this value and has used industry relevance as a core criterion when selecting research topics. The projects were created by consulting industrial partners and all test samples used in the projects were supplied by partners. To increase the impact, MG chose to publish their results at industry-centric conferences, such as IEDM, where leading companies, such as Intel, announce their latest breakthroughs. The knowledge gained through this industry-centric research approach enables the MG to provide a service to the industry in terms of:

(W1) The predicative modelling

Early works from some research groups verified their device-ageing models by showing that the models can fit test data well. This, however, did not deliver the original mission of the modelling: to predict device and circuit performance where test data does not exist. MG determined to take up this challenge and qualified their model by its capability to predict device performance under real use conditions [R3]. This has attracted the attention of industry and the model has been used to:

I. Qualify new processes and materials by using the model to predict device lifetime:

Ever since the invention of integrated circuits in 1958, the intensive competition has driven the industry to develop a new process every 1.5~2 years. Before one process can make its commercial debut, the industry standard requires a device lifetime of 10 years. This requires prediction, as it is impractical to test devices for that long. The MG’s predictive model has been used to qualify new processes [S1, S2 (Section 5)].

S1 is a partner of the EPSRC-funded projects and supplied some of the test samples used by the projects. The research results were disseminated directly to it through progress meetings. Two members of MG joined S1 to work on process qualification: Dr MB Zahid in 2008 and Dr B Tang in 2016.

S2 is an international chip foundry. After MG presented the AG model at the 2013 IEEE International Electron Devices Meeting (IEDM), S2 invited members of MG to present the model to the company’s test engineers in 2014. After the presentation, the company decided to adopt the model. This involves changing test procedure and data analysis to improve the accuracy of device lifetime estimation. The company’s lawyers did not allow the company to provide a financial figure on the benefit of the model to the company.

In addition to S1 and S2, the model has received an increasingly wide attention and members of MG have been invited and funded to deliver tutorials to train test engineers on how to implement the model. Over 500 engineers have taken part in the training so far. The latest tutorial was delivered at the 26th IEEE International Symposium on the Physical and Failure Analysis (IPFA) of Integrated Circuits, Qingdao, July 2019, with over 100 attendees [S3].

II. Product Design Kit (PDK)

The modern microelectronic industry has some companies, such as ARM, specializing in design and others, such as TSMC, focusing on fabrication. The bridge between them is PDK. The ‘First Silicon Success’ relies on the accuracy of models used in PDK and the discrepancy between models and silicon performance is a major challenge to the industry. The research and models of MG have been used to develop reliability- and variability-aware PDKs [S4, S5]. These PDKs allow designers to take the reliability and time-dependent device-to-device variation into account when verifying their circuits, which in

turn not only increases the 'First Silicon Success', but also optimizes the performance of designed circuits in term of power, speed, and cost.

Semiwise [S4] is a start-up, while S5 is a prime international supplier of Electron Design Automation (EDA) software. S5 is a partner in the EPSRC projects [G4, G6] and at the end of project G4, the post-doctoral researcher, Dr M Duan, joined S5 in 2018 to work on variability-aware PDK. The collaboration with S4 and S5 is further strengthened through the award of the joint EPSRC project ("Realistic fault modelling to enable optimization of low power IoT and Cognitive fault-tolerant computing systems", EP/T026022/1, £487k) in 2020.

(W2) Embedding test techniques into commercial instruments

Based on commercial instruments, MG developed a number of advanced characterisation techniques that require technique-specific programs and hardware setups. MG realised that these programs and setups were not available to other users of the same instruments, as MG were invited by a project partner to implement the technique for their laboratory [S1].

After this experience, MG contacted the instrument supplier and explored embedding these techniques into their instruments as a module. The company then invited MG to visit their research and development centre in Ohio, USA, followed by the company visiting Liverpool John Moores University. The module has been jointly developed and embedded into the supplier's most advanced semiconductor parameter analyser, KEITHLEY 4200, and shipped to the customers. MG worked together with the supplier to prepare the module's user manual. In addition, MG was invited and funded to train test engineers at the workshops organized by the supplier [S6]. This collaboration started in 2012 and is on-going, as more techniques have been added to the module when they are developed by MG.

Since 2017, over 4,000 engineers have taken part in the training. The Company could not tell MG how many customers bought the instrument because of this test module. What they can say is that, at September 2019, 3145 copies of the module were shipped together with the instrument to world-wide customers [S6]. To continue the collaboration and add more techniques to the module, the Company offered a PhD studentship to MG [S7].

(W3) Contributing to development of new technologies

As transistors are downscaled to nano-meters, the cost of developing future technologies becomes so expensive that even the sector's largest companies, such as Intel, cannot afford to do everything on their own. To share the cost, the industry has formed a consortium, based at IMEC, Belgium, whose members include Intel (US), ARM (UK), Micron (US), Samsung (Korea), Toshiba (Japan) and TSMC (Taiwan). Each company has its own assignees based at IMEC. Every six months, there is a partner technical week (PTW) to review the progress of the R&D work.

The cost of fabricating the industry-relevant nano-meter transistors is well beyond the reach of MG. To contribute to this world-wide effort to develop future generation technologies that impact the daily life of society, MG's strategy has been to collaborate with this industrial consortium and to focus on the qualification of new processes, materials and devices sourced from the consortium.

To strengthen the link with the consortium, MG has one researcher based at IMEC, who takes part in the daily R&D activities of the consortium. This offers a direct bridge between MG and the consortium. The issues to be addressed and the test samples needed by MG are co-identified with the researchers at IMEC. The results are disseminated directly to the consortium through MG's researcher at IMEC. The MG's works have impacted the Consortium's development work in terms of material selection, structure evaluation, and performance optimization [S8]. For example, one joint paper published at 2019 IEDM conference is entitled "Endurance improvement of more than five orders in GexSe1-x OTS selectors by using a novel refreshing program scheme" [R4].

The value of this collaboration has been recognized by IMEC and IMEC has supported the research at LJMU through a rolling contract of Euro100k p.a. for over 20 years [G7]. To the best of MG's knowledge, LJMU is the only UK university that IMEC has supported continuously in this way for over two decades. LJMU is also the only UK university that has been regularly invited to give presentations to the Consortium at its 'partner technical week' meetings. It is a privilege for

MG to work together with THE world leading consortium at the forefront of developing new technology. This has allowed MG to punch well above its weight. The collaboration goes from strength to strength, initially in the area of logic devices and now also in memory devices.

(W4) Defect-based True Random Number Generator and its commercialization

The three key issues identified for IoT are security, cost, and power consumption. Random Numbers are required in cryptography and authentication and their generator is an essential component of security systems. The algorithm-based software generators used in some security systems are not truly random and are vulnerable to attack. The True Random Number Generator (TRNG) harvests the randomness of natural phenomena in hardware without using an algorithm.

MG has gained an in-depth knowledge of defects in transistors, whose charging-discharging produces random telegraph noise. Although noise is unwanted for normal electronic circuits, MG innovatively harvested its randomness to design and build a TRNG, which is 10 times faster than the TRNG proposed by early works [R6]. The events comprising this impact are outlined in chronological order below:

- MG submitted a paper on its TRNG to the 2018 Symposium on VLSI technology. The conference organizer not only accepted the paper [R6], but also invited and funded MG to demonstrate the TRNG to the conference attendees, along with the demonstrations by Intel Corporation and Panasonic Corporation [S9].
- MG applied for, and was awarded a grant by Innovate UK to develop a proto-type product for its TRNG [G8].
- MG was invited to demonstrate its proto-type product at the 2018 International Security Expo in London. A number of companies expressed their interest in the product.
- This led to the award of USA patent (Attorney-Docket-Number: P34923US1).
- Crypta Labs and Secure Technologies Ltd are bidding for the IP for security application in their products [S10].

In summary, to maximize the significance of the impact of its research, MG has chosen to work together with world leaders by providing better models (W1), new test techniques (W2), material/structure optimization (W3), and new product design (W4). This collaboration also led to a wide reach of its impact. For example, by embedding the new technique into the instruments of a prime supplier, it reached the supplier's world-wide customers. The sustainability of MG's approach has been demonstrated by the continuous collaboration and by the partnership in the EPSRC projects with these leading organizations over the last two decades.

5. Sources to corroborate the impact

[S1] R&D manager - Device Reliability and Electrical Characterization group at IMEC, Belgium.

[S2] Reliability Engineering Manager, Semiconductor Manufacturing International Corporation.

[S3] Tutorial in The 26th IEEE International Symposium on the Physical and Failure Analysis

(IPFA) of Integrated Circuits, 2019.

[S4] Chairman, Semiwise, UK.

[S5] Design Manager, Synopsys.

[S6] Marketing Manager, Tektronix.

[S7] General Manager of Keithley Instruments, USA.

[S8] VP Memory & Storage, IMEC, Belgium.

[S9] Process Integration Manager, Texas Instruments, Texas, United States; Group Leader, Central Research Laboratory, Hitachi, Tokyo, Japan.

[S10] Chief Executive Officer of Crypta Labs and Director of Secure Technologies Ltd.