Institution: University of Greenwich

Unit of Assessment: 12 - Engineering

Title of case study: Design for reliability: Transforming reliability, quality, efficiency and cost savings in design and production for the high value electronics industry, and informing industry standards across the globe

Period when the underpinning research was undertaken: Jan 2000 – Dec 2020

Details of staff conducting the underpinning research from the submitting unit:

Name(s):	Role(s) (e.g. job title):	Period(s) employed by submitting HEI:
Christopher Bailey	Professor	01/12/1990 – present
Stoyan Stoyanov	Reader	01/05/1999 – present
Hua Lu	Reader	16/10/1995 – 01/02/2021
Chunyan Yin	Lecturer	01/01/2007 – 31/08/2019
Timothy Tilford	Senior Lecturer	05/10/2004 – present

Period when the claimed impact occurred: Aug 2013 – July 2020

Is this case study continued from a case study submitted in 2014? N

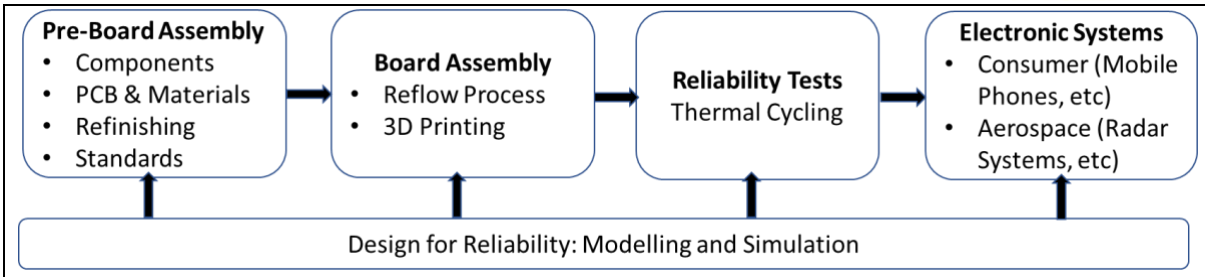
1. Summary of the impact

The Computational Mechanics and Reliability Group (CMRG) at University of Greenwich develops state-of-the-art numerical models to estimate when and how innovative, high-reliability, and high-value electronics systems will fail. The work's impacts relate to economic impacts (£30,000,000) for electronics companies in the aerospace sector, such as Leonardo and Micross, through better-printed circuit board assembly designs that meet these high value-added electronic systems' reliability requirements. Our work has also led Microsemi to adopt 3D printing in their electronics manufacturing processes, reducing costs and time to market by 10%, and reducing material wastage by 2-3%. Additionally, we have extended our knowledge through the IEEE (the world's largest technology professional society), impacting the development of new standards and influencing a technology roadmap for practitioners in the worldwide electronics sector.

2. Underpinning research

The research activity at the University of Greenwich in Electronics Packaging, led by **Professor Chris Bailey**, began in 1998. Electronics packaging involves selecting components (semiconductors, bare printed circuit boards, etc.), materials, and assembly processes to manufacture assembled printed circuit boards and then to test these boards and then assemble these boards into electronics systems that range from mobile phones to avionics radar systems. A key challenge for the electronics industry is to ensure that the design of these assembled printed circuit boards meet end-user requirements in terms of their reliability for different market applications.

Since 2000, CMRG has focused its research activities on developing modelling and simulation techniques to support Design for Reliability (DfR) by predicting the mechanical behaviour in these electronic assemblies when subjected to changes in temperature during pre-board assembly, board assembly, reliability testing, and when in-service as an electronic system (in a mobile phone, aircraft, etc.). The research methodologies are based on finite element methods using high-performance computing (HPC) to predict the physics taking place across the four stages of product development as detailed in the figure below. The developed modelling techniques provide the ability to support DfR and predict the magnitudes of changes in temperature, stress, damage (cracks, etc) in all the materials, making up an assembled printed circuit board from the pre-board assembly to the final electronic system.



Our early research (2000-2004) was supported by three EPSRC projects in collaboration with BAE Systems, Rolls Royce, Celestica Ltd, Multicore solders, MBDA, Alpha Metals, and DEK. This research undertaken by CMRG developed the first multi-physics models to predict the changes in temperature, stress, and damage during the reflow process and subsequent reliability testing of Flip-Chip electronic components [**3.1**]. From 2004-2019, CMRG has extended its modelling expertise to other electronic components, including Ball Grid Arrays (BGA) and Quad Flat No-Leads (QFN); refinishing processes (e.g. hot-solder dip, and laser deballing/re-balling); novel board assembly processes such as 3D Printing; reliability test environments (aerospace); and health monitoring (prognostics) of electronic systems.

In 2004, CMRG started its long-term collaboration with Leonardo (ex BAe Systems Avionics). Using component, materials, and thermal profiles (test and in-service) data from Leonardo, CMRG extended its flip-chip models to predict the thermo-mechanical behaviour of BGA components. These newly developed models predict the thermally induced fatigue (and associated cracks) in the solder joints when the assembled BGA component is subjected to these thermal profiles. The models confirmed that the location of failure predicted in a reliability test would be the same as that seen when the electronic assembly is used in an aircraft environment. As with the flip-chip components, our models also identified printed circuit board (PCB) and underfill material properties to ensure the assembled PCB meets the aerospace reliability requirements for 25 years of life within an aircraft environment [**3.2**].

From 2004-2019, funded by EPSRC, DTI, EU, US Govt, and consultancy projects with Industry, CMRG extended its modelling capabilities to predict the reliability of many other electronic component constructions and assembled PCB's. For the aerospace sector, the research challenge is to use low-cost commercial electronic components. From 2011-2019, CMRG collaborated with industry partners including Leonardo, Rolls Royce, Micross Semiconductors, Cassidian (Germany), and General Dynamics (USA). Using manufacturing process data provided by Micross Semiconductors and Leonardo's component data, our first project developed the first thermo-mechanical finite element model of the pre-board assembly hot-solder dip refinishing process. The developed models' results demonstrated that the electronic components' exposure to the temperatures induced by the refinishing process would not result in damage to the component [**3.3**].

From 2014-19, we extended our modelling capability to complex electronic component constructions such as QFN's and Micro-BGA's. Using materials data and component construction data from Leonardo, these models predicted the physics that govern the fatigue damage of the assembled PCB's that these components are mounted to during reliability testing. Key findings include the thermo-mechanical effect that materials such as conformal coatings have on these PCB assemblies' reliability and identified specific material properties that would ensure that the aerospace reliability specifications are met [**3.4**].

The benefits of 3D printing for the electronics industry is its ability to design, manufacture, and assemble complex and unique printed circuit board designs with complex shapes and non-planar geometry at low cost and much less material wastage compared to traditional reflow assembly. Funded by the EU (from 2013-2017), and in collaboration with industry partners such as Microsemi, who provided materials and component data, we extended our board assembly modelling techniques to predict the thermo-mechanical behaviour of conductive and non-conductive materials printed using a 3D printing process. Key findings included the developed models' ability to predict the residual stresses during the printing process and identify suitable

material properties and printing process parameters that ensured the fabricated printed circuit boards meet the reliability requirements for the relevant electronic system [**3.5**].

3. References to the research

1. **Bailey, C**., **Lu, H**., Wheeler, D. "*Computational modelling techniques for reliability of electronic components on printed circuit boards*". Applied Numerical Mathematics, 40 (1-2), pp. 101-117, (2002). https://doi.org/10.1016/S0168-9274(01)00065-4
2. **Stoyanov, S**., **Bailey, C**., Mackay, W., Jibb, D., and Gregson C. "*Lifetime assessment of electronic components for high reliability aerospace applications*". *Proceedings of 6th Electronics Packaging Technology Conference (EPTC 2004) (IEEE Cat. No.04EX971)*, Singapore, pp. 324-32, (2004). http://dx.doi.org/10.1109/EPTC.2004.1396627
3. **Stoyanov, S**., **Bailey, C**. "*Modelling the impact of refinishing processes on COTS components for use in aerospace applications*". Microelectronics Reliability, Volume 55, Issues 9–10, 2015, Pages 1271-1279, (2015). https://doi.org/10.1016/j.microrel.2015.07.030
4. **Yin, C**., **Stoyanov, S.**, **Bailey, C**. and Stewart, P. "*Thermomechanical Analysis of Conformally Coated QFNs for High-Reliability Applications"*. IEEE Transactions on Components, Packaging and Manufacturing Technology, 9(11), pp.2210-2218, (2019). https://doi.org/10.1109/TCPMT.2019.2925874 ***[REF2 Submission - Identifier 24734]***
5. **Tilford, T.**, **Stoyanov, S.**, Braun, J., Janhsen, J.C., Burgard, M., Birch, R., **Bailey, C**. "*Design, manufacture and test for reliable 3D printed electronics packaging".* Microelectronics Reliability, 85, pp. 109-117, (2018). https://doi.org/10.1016/j.microrel.2018.04.008 ***[REF2 Submission - Identifier 20182]***

Quality Indicators: Examples of Peer Reviewed Funding

a) *Lead-Free Soldering for Flip-Chip Assembly Applications;* EPSRC Standard Research; PI **Bailey**; Grant (GR/N14095/01); (Apr 2000 – Sep 2002); Value £110,172. Supported the research developments reported in [**3.1**] (above). This project was in collaboration with industry partners: Celestica, ITRI Ltd, MBDA and Multicore Solders.

b) *Component Attach Assessment and Integrity Analysis*; PI **Bailey**; US Gov/General Dynamics Grant: HQ727-16-D-0003; (Oct 2013 – Sep 2018); Value £594,573. Supported research developments reported in [**3.3**] and [**3.4**] (above).

c) *NextFactory;* EU-FP7 project (ID: 608985); UoG PI **Bailey**; (Sep 2013 – Aug 2017); Value £3,965,172 (£350,000 to UoG). This project supported the research reported in [**3.5**] (above). The research reported also received the best paper award at the Fraunhofer Direct Digital Manufacturing Conference (DDMC), Berlin, 2016.

4. Details of the impact

CMRG has been developing DfR modelling techniques since early 2000's. Our research has been widely disseminated, with over 400 academic publications on the topic. However, our primary means to transition the knowledge developed through to direct industrial impact is through our partnerships with many international major electronics companies. Industrial partners adopting our DfR technologies can develop electronics systems with improved reliability and reduced in-service failures. Product failures have costs, both fiscal and reputational. For example, the costs of each reliability test (which can run over a period of 6 months) is in-excess of £100,000 and the cost of a product failure in the field can run into £M's.

Implementation of UoG research at Leonardo has led to financial impacts. Leonardo Spa, based in Edinburgh, employs 2,000 people and specialises in the provision of multi surveillance radars and countermeasures systems. It produces world-leading technology, including Captor Radar for the Typhoon aircraft. The ability to develop and manufacture this equipment on-shore is of strategic importance to the UK, allowing the Ministry of Defence (MOD) to operate without other nation-states' intervention and maintain an operational advantage over potential adversaries.

The transfer of knowledge between the CMRG and Leonardo occurred through direct consultancy in 2004-2005 and 2018-2019, and through collaboration on US Government funded projects throughout 2011-2018. As per the contracts, CMRG provided quarterly reports to the funder and Leonardo, and meetings took place at the company premises to discuss the results from the models. CMRG model predictions for different components [**3.2 & 3.4**] were successfully implemented into radar signal processors, where each processor has a value of the order of £600,000 and the Radar itself has a value of the order of £3,000,000. From 2014 – 31st July, 2020, the results from the models developed by CMRG has informed Leonardo's design protocols and manufacturing standards, and this has removed greater than £30,000,000 of design and qualification risks by ensuring the right materials and assembly processes are used, hence significantly reducing the number of reliability tests**.** The distinct and material contributions made by CMRG to the impacts listed above are confirmed by the University & Emerging Technologies Manager at Leonardo, who states "*the results and knowledge generated from your research has been extremely successful in informing Leonardo's design protocols and manufacturing standards, providing significant benefits to us, our suppliers, and customers globally including our major contracts with Governments in the UK, Italy, Spain, and Germany,*" [**5.1**].

Research by UoG academics helped Micross and Leonardo gain greater insight into refinishing process and secure significant annual growth in this service. Micross Semiconductors is a US company whose refinishing process is used by the high-reliability electronics sector (including Leonardo). From 2011-2014, CMRG worked closely with Micross and Leonardo on a US Government funded project to develop models of the hot-solder dip refinishing process [**3.3**]. Knowledge transfer between CMRG and these companies took place through quarterly reports and meetings at the Crew, UK, Micross facility. The results from the models of 23 electronic component types supported Micross and its customer Leonardo in gaining a greater insight into the thermo-mechanical behaviour of the components when subjected to this refinishing process, providing more guidance than found in the current GEIA-STD-005-2 standard. The results helped Micross secure significant growth in this service throughout the period 2014 - July 31st, 2020. For example, the University & Emerging Technologies Manager at Leonardo states "*computational models developed by your team for the Hot Solder Dipping process – a service provided by Micross Semiconductors – helped Leonardo successfully assess the behaviour of our electronic components when subjected to this refinishing process"* [**5.1**] and the Product Line Manager at Micross states "*the modelling work undertaken at Greenwich has helped us gain a clear insight into to the refinishing process supporting us to deliver product of the highest standard to our worldwide customer base,"* [**5.2**].

UoG research fed into Microsemi's assessment of 3D-Printing for electronics packaging resulting in reductions in material wastage and cost saving benefits. Microsemi (now Microchip) is a US company with facilities worldwide, including its Advanced Electronic Packaging facility in Caldicot, Wales, UK, which offers a comprehensive portfolio of semiconductor and electronic systems solutions for communications, defence and security, aerospace, and industrial markets. During the period 2013-2017, CMRG collaborated with MicroSemi on the EU-Funded project NextFactory. The models developed by CMRG for the 3D-Printing process during this project provided significant insights into the feasibility of MicroSemi adopting this process and addressing the key technical barrier of residual stresses in the fabricated parts. Based on the results from the NextFactory project (including the modelling undertaken by CMRG [**3.5**]), in 2019, Microsemi purchased a 3D printer to support its strategy in driving the next generation of 3D electronics systems miniaturization. During the period to 31st July, 2020, this led to a 2-3% reduction in material wastage compared to traditional reflow-based board assembly processes and a decrease in time to market and cost savings of 10%. The ability to design genuinely 3D print printed electronic products has also opened-up new product lines for the company [**5.3**]. Technical staff engineer at Microchip states, "*the results from your models have supported our assessment of this manufacturing process and in Summer 2019 the company purchased a 3D printer to supplement our existing stencil printers. This printer is now used with our design and manufacturing departments for prototype evaluation and tooling for several high-value export products to North America and Europe".*

UoG's work into modelling and simulation made significant contributions to IEEE Standards and Roadmapping. The IEEE is the world's largest professional body with over 420,000 members globally. Most of the world's major electronics companies are members of IEEE. As part of its relationship with IEEE and the high-quality work in modelling and simulation produced over the years, CMRG was invited to participate in the development of the Heterogeneous Integration Roadmap (HIR) in 2016 [**5.4**]. The HIR roadmap provides state-of-the-art / best practice in Electronics Packaging and its drive to produce the next generation of 3D heterogeneous electronic systems. It contains the chapter Modelling & Simulation, which is led by CMRG. This involved **Professor Bailey** chairing the Technical Working Group for this chapter bringing together experts in modelling and simulation worldwide to contribute to the chapter's contents, which contains material from CMRG – particularly our research into multi-physics modelling and design for reliability. From 2019-July 31st, 2020, the HIR roadmap has been downloaded 24,197 times by engineers at electronics companies and research organisations globally. This is confirmed by the IEEE [**5.5**] and the roadmap's manager and the Chief Scientific Advisor of ASE group, the world's largest semiconductor assembly & test company states: "*The modelling & simulation research undertaken by the Greenwich team provided significant contributions to the Heterogeneous Integration Roadmap. This roadmap is now guiding the worldwide electronics industry to progress beyond 56-years of 'Moore's Law' (transistor and economics scaling) through innovations in advanced electronics packaging and heterogeneous integration".* [**5.4**].

From 2012-2017, **Professor Bailey** also contributed to the IEEE Standard P1856 (Standard Framework for Prognostics and Health Management of Electronic Systems) as part of its development working group. This standard provides the electronics industry with best practice guidance on the use of techniques (including modelling and simulation) for prognostics in electronic systems. The standard and the roadmap are both conduits to transition the group's DfR expertise into improvements in the reliability of products of a great many companies globally. The manager of the standard confirms: "*The research undertaken by the Greenwich team contributed to this important standard for the electronics industry to address the latest techniques in Prognostics and Health Management for electronics systems across the electronics ecosystem from consumer electronics to renewable energy to medical devices to aerospace"* [**5.6**].

5. Sources to corroborate the impact

1. Statement from Leonardo corroborates the impact of our research for predicting the reliability of radar electronic systems.
2. Statement from Micross corroborates the impact of our research for predicting the thermo-mechanical behaviour of the Hot Solder Dipping process.
3. Statement from Microsemi corroborates the impact of our research for predicting the residual stresses in the 3D-printing process.
4. (a) Details of the roadmap can be found at: https://eps.ieee.org/images/files/HIR_2019/HIR1_ch14_sim.pdf;
   (b) Testimonial: Chair of the IEEE Roadmap.
5. Testimonial: Executive Director, EPS, IEEE corroborates the number of downloads of the first edition of the HIR roadmap during the period 2019-July 31st 2020.
6. (a) IEEE Standard P1856 – Standard Framework for Prognostics and Health Management of Electronic Systems, https://ieeexplore.ieee.org/document/7564361 University of Greenwich is a member of the working group (based on its research in reliability of electronics systems).
   (b) Testimonial: Chair of this IEEE Standard.